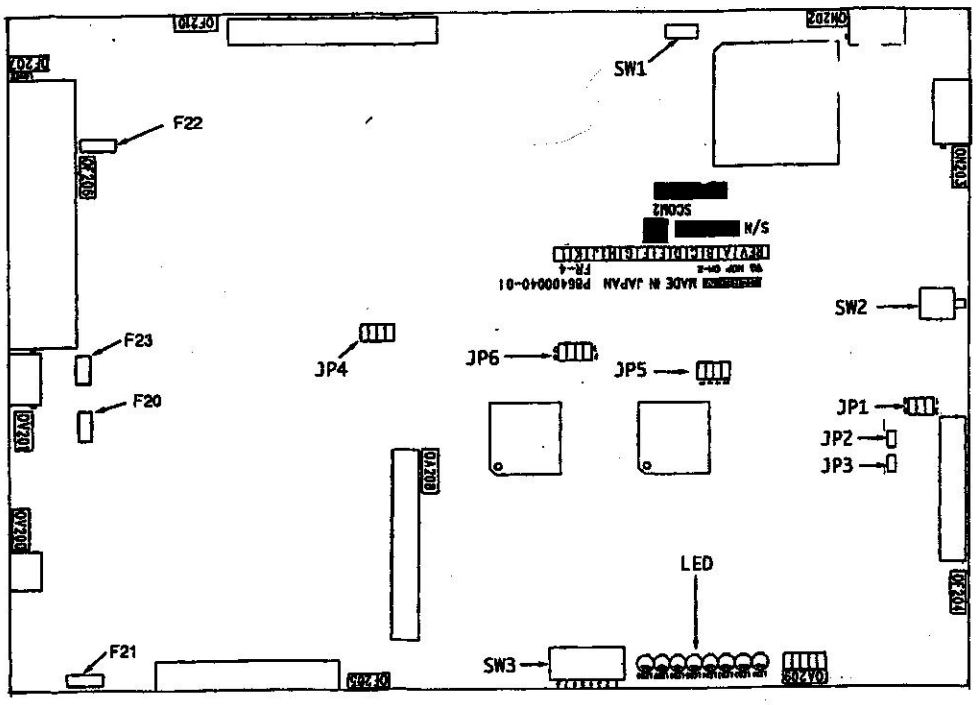
(4 1 — 2) SCOM board settings



【List of fuses】

Fuse No.	Current (A)	Model No.	PART CODE	Rating	Related Motor
F20	7.0			7A	Protection of the board
F21	1.0	218001	60200108	1A	Term Power (SCSI)
F22	1.0	218001	60200108	1A	H D D 1
F23	1.0	218001	60200108	1A	H D D 2

【List of LED functions】

LED No.	Light-up timing	Turn-off timing
1	When data for one separation is output	When transferring to the next exposure sequence
2	Unused	
3	When the rear memory FIFO data does not follow the READ signal and an error signal is issued	When transferring to the next exposure sequence
4	When a command interrupting exposure is sent from the ENGINE side during the exposure (Exp. When the STOP key is pressed)	When transferring to the next exposure sequence
5	When the Page signal is activated (The "Enable bit" is turned ON.)	When the Page signal is negated (The "Enable bit" is turned OFF.)
6	When the HDD#0-SPC interrupt processing is started	When the HDD#0-SPC interrupt processing is finished
7	When the HDD#1-SPC interrupt processing is started	When the HDD#1-SPC interrupt processing is finished
8	When the HOST-SPC interrupt processing is started	When the HOST-SPC interrupt processing is finished

【Table of jumper settings】

Jumper	Description
J P1	Setting should be changed depending on the EPROM capacity. (1M word or 4M word) Shorted (only1-2): 1M word Shorted (3-4 and 5-6) : 4M word Normal setting : Shorted (3-4 and 5-6)
J P 2	Setting should be changed depending on the FlashROM capacity. (8M bit or 16M bit) Open : 8M bit Shorted : 16M bit Normal setting : Open (lower byte)
J P 3	Setting should be changed depending on the FlashROM capacity. (8M bit or 16M bit) Open : 8M bit Shorted : 16M bit Normal setting : Open (upper byte)
J P 4	FIFO controller setting for the external DRAM Front memory FIFO-A 1-2 (VSEL0) 3-4 (VSEL1) : External DRAM memory capacity Shorted Shorted : 256K word Shorted Open : 1M word Open Shorted : 4M word Open Open : 16M word 5-6 (TSEL0) 7-8 (TSEL1) : Low address multiplexer Shorted Shorted : 9 bit Shorted Open : 10 bit Open Shorted : 11 bit Open Open : 12 bit Normal setting : Open (1-2 and 5-6) : Shorted (3-4 and 7-8)
J P 5	FIFO controller setting for the external DRAM Rear memory FIFO 1-2 (VSEL0) 3-4 (VSEL1) : External DRAM memory capacity Shorted Shorted : 256K word Shorted Open : 1M word Open Shorted : 4M word Open Open : 16M word 5-6 (TSEL0) 7-8 (TSEL1) : Low address multiplexer Shorted Shorted : 9 bit Shorted Open : 10 bit Open Shorted : 11 bit Open Open : 12 bit Normal setting : Open (1-2 and 5-6) : Shorted (3-4 and 7-8)
J P 6	FIFO controller setting for the external DRAM Front memory FIFO-B 1-2 (VSEL0) 3-4 (VSEL1) : External DRAM memory capacity Shorted Shorted : 256K word Shorted Open : 1M word Open Shorted : 4M word Open Open : 16M word 5-6 (TSEL0) 3-4 (TSEL1) : Low address mutiplexer Shorted Shorted : 9 bit Shorted Open : 10 bit Open Shorted : 11 bit Open Open : 12 bit Normal setting : Open (1-2 and 5-6) : Shorted (3-4 and 7-8)

【Table of DIPSW settings】

DIPSW No.	Description
1	Activates LED blinking.
2	Activates forced download mode or writing to the Flash ROM.
3 ~ 6	Unused.
7	Sets the active terminator OFF. (upper byte)
8	Sets the active terminator OFF. (lower byte and control signal)

* Normal setting is all numbers OFF. When a DIPSW setting is turned ON, the conditions as noted above will be activated.

【Table of SW1 settings】

No.	Description
1	Master mode of the CPU. This is the normal mode with bus permission. Normally, set this to ON.
3	Slave mode of the CPU. This is the mode which releases bus permission.